IN THE SPECIFICATION

Please replace the paragraph starting at line 28 of Page 14 with the following amended paragraph:

Figure 2 shows a multicore processor implementing the logical arrangement of Figure 1, again by way only of an example. The multicore processor of Figure 2 employs a plurality of the processing resources 150, each connected via a system interconnect 160. In one embodiment, at least one of the plurality of processing resources 150 is a master processing unit. The system interconnect 160 communicates in turn with the system management controller 130 via input interfaces 100, and output interfaces 110. In the example of Figure 2 the system interconnect 160 is laid out as a traditional central bus which connects each of the processing resources 150 with one another and with the controller 130, and also with the shared system resources such as a system memory 140. Interfacing with the memory 140 may be achieved via any one of a number of currently available interface technologies. The memory may consist of any of the currently available central computer memory technologies, for example Dynamic Random Access Memory (DRAM), or Double Data Rate Random Access Memory (DDR RAM).